HgTe/CdTe heterojunctions: A lattice-matched Schottky barrier structure

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HgTe-CdTe lattice-matched heterojunctions were formed by the epitaxial growth of HgTe on CdTe substrates using a low-temperature metal organic chemical vapor deposition technique. These heterojunctions combine features of the Schottky barrier structure, due to the high carrier concentrations found in the semimetallic HgTe, with the structural perfection present in a lattice-matched heterojunction. The measured Schottky barrier height varied from 0.65 to 0.92 eV depending on the details of the heterojunction growth procedure used. This dependence may be due to the formation of an inversion layer in the CdTe at the interface. Presence of such an inversion layer suggests that the valence band discontinuity between HgTe and CdTe is small, in agreement with previous theoretical estimates.

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I. INTRODUCTION

The study of the HgTe-CdTe heterojunction system is of both technical and scientific interest. Most of the current interest in this system stems from its similarity to the heterojunction formed by the epitaxial growth of $Hg_xCd_{1-x}Te$ on CdTe substrates. HgTe and CdTe are completely miscible, forming a solid solution at all compositions of $Hg_xCd_{1-x}Te$. Since the lattice parameters of HgTe and CdTe are nearly equal ($\Delta a/a = 0.003$), approximately lattice-matched epitaxial growth of $Hg_xCd_{1-x}Te$ for all values of x may be obtained on CdTe substrates. $Hg_xCd_{1-x}Te$, at high values of $x(x > 0.7)$, is an important material for use in infrared detectors and imaging arrays. The band gap of this material may be varied with composition over a wide spectral range from near the visible ($x \simeq 0$) to over 30 μm ($x > 0.80$).[1] The heterojunction consisting of HgTe on CdTe may have a number of applications in its own right. Calculations on superlattices composed of alternating ultrathin layers of HgTe and CdTe have suggested desirable optical and electrical properties.[2] The realization of such properties depends, however, on the existence of a small valence band discontinuity between HgTe and CdTe. A further application of HgTe epitaxial growths results from the higher Schottky barrier they can afford, compared to an elemental metal, on CdTe.

This particular heterojunction may also provide some insight into the mechanism of Schottky barrier formation. The group of HgX/CdX heterojunctions, where X = S, Se, or Te, are rather unique in resembling a Schottky barrier, due to the high carrier concentrations present in the semimetallic Hg chalcogenides, and yet affording the structural perfection present in lattice-matched heterojunctions. Since HgTe and CdTe are similar in their chemistry and physical structure, the study of this heterojunction system provides a rather ideal Schottky barrier structure free of the structural and chemical complexities found in most metal-semiconductor contacts. Furthermore, the predictions of the Schottky barrier height ϕ, based on simplified models of a heterojunction, have been made, indicating a rather large barrier of $\phi \simeq E_{gap} = 1.5$ eV, the band gap of CdTe. The actual barrier height determined on such structures in the present study, however, is substantially less, ranging from 0.65 to 0.92 eV depending on the pregrowth annealing conditions used in preparing the CdTe substrate surface. The discrepancy between the predicted and observed values of the band discontinuities along with this dependence of the barrier height on growth conditions will be discussed in terms of a possible model of this heterojunction system.

II. BAND DISCONTINUITIES, HETEROJUNCTION GROWTH CONSIDERATIONS

The electrical properties of the ideal heterojunction are largely determined by the relative positions of the conduction and valence bands at the interface. If the band gaps of the two semiconductors differ, the heterojunction will exhibit discontinuities in one or both of the bands at the heterojunction interface. In this study, we hoped to determine these band discontinuities between HgTe and CdTe.

There have been several estimates of the band discontinuities at the HgTe/CdTe heterojunction. The simple model of Anderson[3] predicts that the valence band discontinuity at the heterojunction interface is equal to the difference in the ionization potentials of the semiconductors or, equivalently stated, the conduction band discontinuity is equal to the difference in electron affinities. The conduction band discontinuity of the HgTe/n-CdTe heterojunction would then be the Schottky barrier height of this structure, and the two terms, conduction band discontinuity and Schottky barrier height, will be used interchangeably further in this paper. In support of this model, experimental values of the ionization potential measured on CdTe and HgTe yield similar values.[4]

The valence band discontinuity present in the HgTe/CdTe heterojunction can also be predicted by a meth-

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od developed by Harrison.[5] A relative valence band maximum (ionization potential) is assigned each material by a simplified tight binding approach. The valence band discontinuity present at a given heterojunction is then obtained by the subtraction of the two assigned values of the valence band maxima. This theoretical method successfully predicts the proper band discontinuities in a number of heterojunction systems such as Ge on GaAs and InP on CdS.[5] When applied to the present system, a valence band discontinuity of less than 0.1 eV is predicted in the case of both HgTe on CdTe and the related heterojunction HgSe on CdSe.

A third prediction is afforded by the phenomenological "common anion" rule. This states that compound semiconductors having the same anion will form an interface with zero valence band discontinuity.[6] Thus, a result very close to Harrison's theory is predicted.

The lattice-matched Schottky barrier, HgSe on CdSe, constitutes a prior test of these predictions and has been studied previously by Best and McCaldin.[7] The measured Schottky barrier height of 0.7 eV is much less than the ~ 1.7 eV band gap of CdSe, which would be predicted for the barrier height by Harrison's theory (and common anion rule). It should be noted, however, that Anderson's model, in view of experimental ionization potentials,[4] agrees much better with experiment. The failure of Harrison's method in the HgSe/CdSe case may possibly be attributed to the fact that CdSe cannot be made p-type. Compensating defects are thought to be created in the material as the Fermi level is pushed to the lower half of the gap. This may prevent the formation of a Schottky barrier height greater than half the band gap in CdSe.[8] This complication does not arise in the case of CdTe, which can be made both p- and n-type. A HgTe on n-CdTe Schottky barrier height, which is approximately equal to the band gap of CdTe, is therefore also predicted by this model.

It should also be noted that the electrical characteristics of the HgSe/CdSe heterojunction depended on the growth procedure.[8] Prior to the HgSe growth, the CdSe substrate was annealed in either a H_2 or Ar ambient in order to remove any damage and surface impurities on the substrate surface. Heterojunctions fabricated on Ar annealed substrates yielded rectifying contacts with the above-mentioned barrier, 0.7 eV. Contacts formed by the growth of HgSe on H_2 annealed CdSe yielded an ohmic characteristic. In this case, the extreme reducing atmosphere was thought to make the surface region of the CdSe highly n-type by the introduction of native donor defects such as Cd interstitials and Se vacancies.[8] This highly doped region would enhance the tunneling current at the junction to a point where rectification is no longer achieved.[9]

The measured band discontinuities can be affected by the compositional grading at the heterojunction interface and, ideally, one would like a perfectly abrupt interface between the CdTe and HgTe. However, interdiffusion between HgTe and CdTe has been found to be quite rapid at low temperatures,[10] which could lead to a reduction in the heterojunction Schottky barrier height. If there is a slow compositional grading between the two materials, the built-in potential resulting from the difference in electron affinities between HgTe and CdTe is screened by mobile charge carriers. The grading of the electron affinity present in an interdiffused heterojunction is analogous to the situation existing at a graded p-n junction.[11]

The band bending in a heterojunction, resulting from the electron affinity difference, will be reduced from that present in an abrupt junction when the interdiffusion distance is of the order of the Debye screening length of the material. Oldham and Milnes have developed a criterion for rectification to occur at a n-n heterojunction formed between two nondegenerate semiconductors.[12] When their criterion is applied to the HgTe-CdTe heterojunction formed in this study, we find that the interdiffusion distance must be less than 1400 Å for rectification. The interdiffusion distance of HgTe and CdTe must be confined to a small fraction of this distance for a negligible decrease in the observed barrier height. Extrapolation of the interdiffusion data, measured at elevated temperatures,[10] yields an interdiffusion distance of 100–300 Å for a typical growth temperature of 325 °C and growth period of 20 min. This short interdiffusion distance ensures that the compositional grading should have a minor effect on the measured barrier height using the model of Oldham and Milnes, though the presence of a degenerate semiconductor, HgTe, in this heterojunction system may require some modifications to this model.

The need to minimize the interdiffusion of HgTe and CdTe was one of the main motivations for using a low-temperature growth technique in this study. The temperatures typically encountered in the LPE growth of $Hg_{1-x}Cd_xTe$ using a Te solvent are 500–600 °C.[13] A growth period of 10 min would lead to an interdiffusion distance, defined as the distance over which the value of x changes from $x = 0.2$ to $x = 0.9$, of over 7000 Å, clearly exceeding the limit for a rectifying junction for doping and band discontinuities similar to those considered in this study. This has also been the case in previous attempts at fabricating the HgTe-CdTe heterojunction.[10]

III. EXPERIMENTAL

The HgTe-CdTe heterojunction was fabricated using a recently developed low-temperature metal organic chemical vapor deposition technique (MOCVD).[14] In this growth technique, epitaxial films of HgTe of good crystalline quality can be grown on CdTe substrates by the reaction of Hg vapor and dimethyl tellurium, $(CH_3)_2Te$, at growth temperatures of 325–350 °C.

Substrates of $\langle 110 \rangle$ CdTe were prepared by cleaving bulk single crystals of CdTe in air. The substrate was annealed in the CVD reactor under a H_2 atmosphere for 30–180 min at typically 325–350 °C prior to the HgTe growth. An alternative annealing procedure consisted of annealing the substrate under a H_2 atmosphere containing Cd vapor. The Cd vapor was supplied by a metallic Cd source. The Cd source temperature was always greater than 321 °C to ensure a molten Cd source, but 2–5 °C lower than substrate temperature preventing the condensation of Cd onto the substrate surface. An annealing step was always found necessary to ensure epitaxial growth of the HgTe. Subsequent to this annealing period, HgTe was then grown on the annealed CdTe surface.

The HgTe layers were first examined by 1.5-MeV helium backscattering and channeling measurements and glancing angle x-ray diffraction. The growth morphology of the layers was examined by scanning electron microscopy (SEM). Secondary ion mass spectrometry (SIMS) was also used to determine changes in the In dopant concentration in the CdTe substrates, due to the pregrowth annealing treatments.

The HgTe-CdTe heterojunctions were also used in a variety of electrical measurements. The samples were first prepared for the electrical measurements by making ohmic contact to the CdTe substrate with In-Ag solder (90% In:10% Ag). Circular areas were defined on the HgTe surface by conventional photolithography techniques. Mesas diode structures were then formed by etching the HgTe layer in 1% Br in methanol. This procedure gave circular diode structures having an area of $1.4–2.0\times 10^{-4}$ cm^2. Contact was made to the HgTe layer by an Au pressure contact. These structures were then used in the subsequent room temperature measurement of the forward bias current voltage characteristic, the diode photoresponse, and the reverse bias capacitance voltage characteristic.

Other Schottky barrier structures on CdTe substrates, Au/n-CdTe, were also prepared in this study. The effects of the annealing procedure on the CdTe substrates could be studied by use of these structures without the complications due to the subsequent growth and interdiffusion of the HgTe. Substrates of In doped CdTe, with $n = 10^{17}$ to 10^{18} cm^{-3}, which had been air cleaved, were annealed in pure H_2 for varying lengths of time at the HgTe growth temperature (~ 330 °C). Gold Schottky barrier structures were made by evaporating Au dots onto the annealed CdTe surface in an ion pumped vacuum system ($< 10^{-6}$ Torr). The I-V and capacitance characteristic on these structures were then measured. Changes in the electrical properties of the near-surface region of the CdTe, as determined from these measurements, could then be correlated with the pregrowth annealing treatment.

IV. RESULTS

The study of the physical structure of the HgTe layers by x-ray diffraction and 1.5 MeV $^4He^+$ backscattering and channeling techniques was given previously in Ref. 14. These studies indicated that the HgTe grew epitaxially on the CdTe substrate and was of good crystalline quality. The surface of the HgTe was generally smooth, exhibiting little or no surface relief.[14] The I-V, C-V, and photoresponse measurements taken on the resulting HgTe-CdTe heterojunction diodes indicate a dependence of the electrical characteristics on the anneal performed on the CdTe substrate preceding HgTe growth.

The forward bias current voltage characteristic was measured over three to four decades of current. The measured characteristic was fitted to an equation of the form

$$J = J_0(e^{qV/nk_BT} - 1), \tag{1}$$

where J is the measured current density at a given applied voltage V and n is the quality factor of the diode. If n is close to unity and J_0 is independent of the applied voltage, the current transport over the electrostatic barrier can be interpreted in terms of Bethe's thermionic emission theory.[15] The reverse saturation current of the diode J_0 is given by this theory as

$$J_0 = A^{**}T^2 e^{-q\phi/k_BT}, \tag{2}$$

where A^{**} is the modified Richardson constant, T is the absolute temperature, and ϕ is the Schottky barrier height. The constant A^{**} is 120 (m_e^*/m_0) in A/cm^2, where m_e^* and m_0 are the effective and free electron mass, respectively. A value of $m_e^*/m_0 = 0.11$ was used here. Two typical I-V characteristics are shown in Fig. 1. The data labeled "H_2 anneal" were taken on a diode where the CdTe substrate was annealed at 335 °C for 30 min in a pure H_2 ambient prior to the growth of the HgTe layer. The data marked "H_2 and Cd vapor anneal" correspond to a structure grown on a CdTe substrate which had a pregrowth anneal of 5–10 min at 338 °C in H_2 gas which had flowed over a molten Cd source held at 337 °C. Substrates receiving a shorter anneal time than 30 min in pure H_2 yielded characteristics which would lie between the two curves shown. Only diodes with a quality factor less than $n \leqslant 1.2$ were investigated further.

The values of the barrier height deduced from these measurements using Eq. (2) indicate a systematic dependence of the barrier height on annealing conditions, with the barrier height being consistently larger for annealing in H_2 and Cd vapor than in H_2 alone. In addition, for substrates annealed in H_2 alone, the measured barrier height decreased continuously with annealing time.

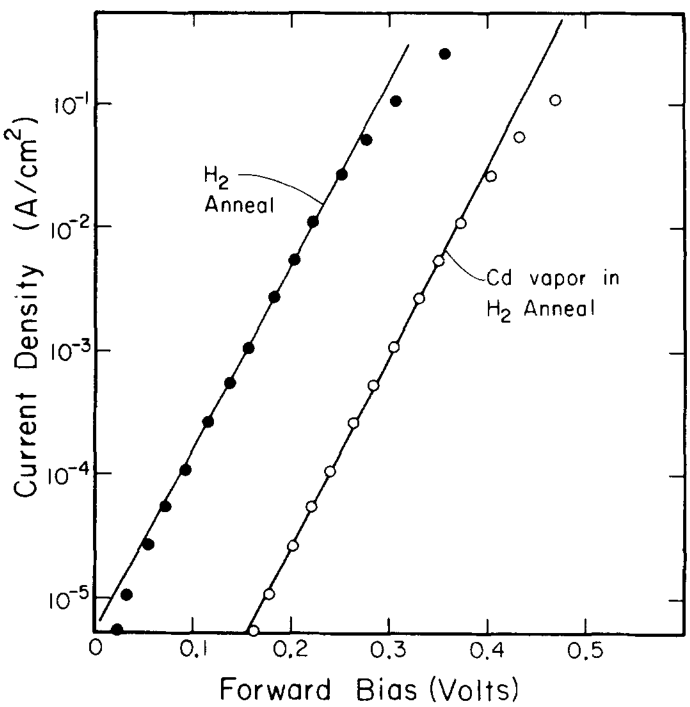

FIG. 1. The forward bias current voltage characteristic of the HgTe/CdTe heterojunction. The heterojunction diodes fabricated on CdTe substrates annealed in a H_2 and Cd vapor ambient exhibited a larger Schottky barrier height than diodes made on H_2 annealed CdTe.

The photoresponse was measured on these structures by illuminating the HgTe-CdTe interface through the CdTe substrate with monochromatic light. The cube root of the photoresponse per incident photon R is shown as a function of photon energy in Fig. 2. The cubic dependence of the photoresponse has been observed for the emission of electrons from a semiconductor into a vacuum[16]:

$$R \propto (h\nu - \phi)^3. \tag{3}$$

The data shown in Fig. 2 were taken on the structures used in Fig. 1. The barrier heights derived from the photoresponse measurements agree well with values deduced from the current voltage measurement. These measurements also indicated an increased barrier height found in samples annealed in H_2 containing Cd vapor.

Capacitance measurements were made on the diode structures as a function of reverse bias voltage using a Boonton capacitance meter (1 MHz, 15-mV test signal). Capacitance data on the structures used in Figs. 1 and 2 are shown in Fig. 3. The data exhibit a deviation from the simple linear behavior usually seen in a Schottky structure. While the capacitance measurements cannot be used to determine a barrier height, they do indicate a spatial variation of the electrical properties of the CdTe with depth into the substrate. These changes develop during the annealing and possibly during the HgTe growth itself.

Systematic trends evident in the measured capacitance characteristics can be correlated with changes in the substrate annealing conditions. As the annealing conditions are changed from the H_2 plus Cd vapor ambient to a pure H_2 ambient, and as the duration of the pure H_2 anneal increases, the capacitance of the structures at zero applied bias decreases. This effect is accompanied by a decrease in the donor concentration as deduced from the slope of the capacitance characteristic dC^{-2}/dV at zero bias, given by

$$N_D = \frac{2}{\epsilon\epsilon_0} \frac{1}{(dC^{-2})/(dV)}, \tag{4}$$

where $\epsilon\epsilon_0$ is the permittivity of the semiconductor and q is the electron charge.[17] The net donor concentration decreases from the preannealed value of 10^{17}–10^{18} per cm^3 to less than 10^{15} cm^3. There is also an increased curvature in the data observed in Fig. 3 with the above sequence of annealing conditions.

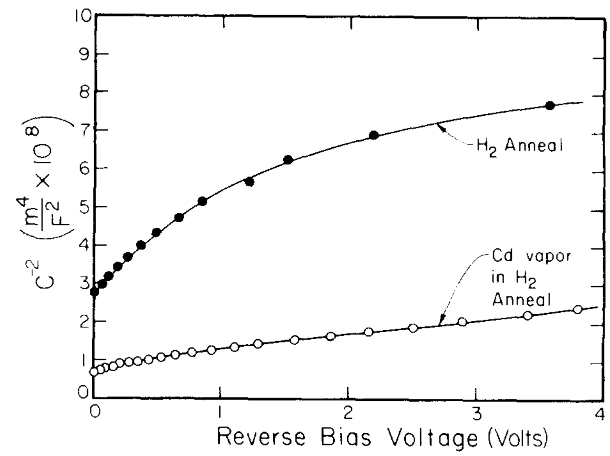

FIG. 3. The reverse bias capacitance-voltage characteristic measured on HgTe/CdTe heterojunction diodes using different pregrowth substrate annealing conditions. The data shown was taken on the samples used in Figs. 1 and 2 with corresponding data point symbols. These curves indicate changes in the electrical properties of the near-surface region (< 1-2 μm) of the CdTe substrate incurred during the pregrowth anneal and HgTe growth.

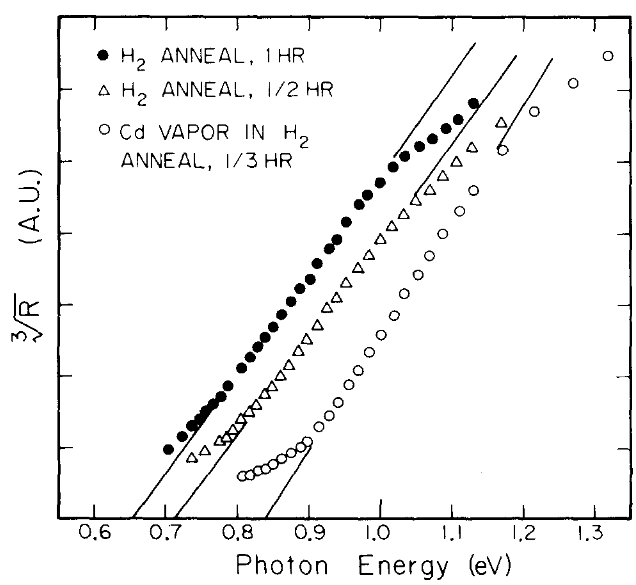

FIG. 2. The photoresponse measurements also exhibited a dependence of the Schottky barrier height on the pregrowth CdTe annealing procedure. The barrier height, uncorrected for the image lowering effect, is given by the intercept on the photon energy axis. The CdTe substrate annealing conditions are indicated on the graph.

The change in barrier height with the net donor concentration deduced from the capacitance characteristic at zero bias is illustrated in Fig. 4. The Cd vapor-annealed substrates yielded the larger barriers and higher deduced donor concentration. The barrier heights given in Fig. 4 are uncorrected for the Schottky or image force lowering effect. Since the sample carrier concentration is 10^{14}–10^{17} cm^{-3} depending on annealing condition, the image lowering would amount to 6–40 meV.

Preliminary SIMS measurements made on CdTe substrates which were both unannealed and annealed in H_2 only for 1 h at 350 °C, indicate changes in the In dopant profile with annealing. The unannealed CdTe substrate had an In dopant concentration of $\sim 10^{18}$ cm^{-3} which is constant in depth. The annealed CdTe exhibited a loss of In from the surface during the anneal as well as some redistribution. The concentration of In near the surface at a depth of $\sim 0.1\,\mu$m was approximately half the bulk doping level. The In concentration increased with depth, becoming equal to In bulk concentration at a depth of $\sim 1.0\,\mu$m. There is also seen in the SIMS results a minor buildup of In, higher than bulk concentration at or near ($< 0.1\,\mu$m) the substrate surface on the annealed samples.

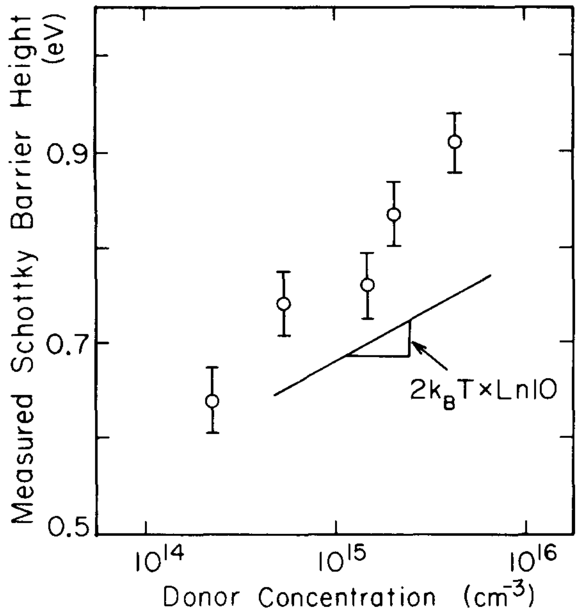

FIG. 4. The measured Schottky barrier height deduced from the I-V and photoresponse measurements were found to increase with the effective donor concentration. An effective donor concentration in the sample was assigned from the value of the slope of the measured capacitance characteristic at zero bias. The barrier height is uncorrected for the image force lowering effect. The carrier concentration in the CdTe was changed by altering the pregrowth annealing procedure. A slope of $2k_BT$ ln 10 given by Eq. (6) is indicated.

Electrical measurements were also made on Au Schottky barriers fabricated on H_2 annealed CdTe substrates. No changes with H_2 annealing conditions were found in the Au Schottky barrier height deduced from the I-V measurement. It should be noted, however, that other annealing procedures have been found to change the Au on CdTe Schottky barrier height. In a previous study, Au-CdTe Schottky barrier devices fabricated on substrate surfaces having a high Cd activity, as compared to the low Cd activity present in the H_2 annealing, produce higher barrier height.[18] Significant changes were seen in the capacitance measurements with the H_2 annealing treatment. Trends similar to those found in the HgTe-CdTe structures are noted in Fig. 5. There is again a decrease in both the zero bias capacitance and donor concentration with the longer annealing times in pure H_2. The Au Schottky barrier structures do, however, have a donor concentration greater than that observed in the HgTe-CdTe structures for identical CdTe substrate annealing conditions. This may indicate that additional compensation or drop in carrier concentration of the CdTe substrate may also be occurring during the HgTe epilayer growth itself.

V. DISCUSSION

The barrier height measured on the HgTe-CdTe heterojunctions varies from 0.65 to 0.92 eV depending on the substrate annealing conditions utilized prior to the HgTe growth. The highest barrier height obtained in this heterojunction appears to be substantially less than that expected for this structure from the simple models of heterojunction behavior. It is therefore important not only to understand the deviations from the simple predictions, but also the dependence of the barrier height on annealing conditions. It would then be hoped that further increases in the barrier height may be possible by additional changes in the growth technique.

This section will first discuss the changes in the electrical properties of the CdTe substrates due to the annealing conditions as observed in the measured capacitance characteristics. Understanding of these anneal induced changes will provide the basis of a model of heterojunction behavior to be presented.

A. Annealing effects in CdTe

Annealing treatments on CdTe carried out under conditions of low Cd activity can produce a drop in the electron concentration in both In-doped and undoped n-type material. This drop in carrier concentration, observed from the capacitance measurements of both the HgTe-CdTe heterojunction and the Au-CdTe Schottky barrier comparison samples, can be attributed to two effects: loss of In dopant from the near-surface regions of the CdTe during the annealing and the introduction of Cd vacancies. These Cd vacancies, which are known acceptors, can complex with In or native defect donors reducing the carrier concentration.[19,20] The equilibrium carrier concentration is then determined by the Cd activity (vapor pressure) and temperature.

The SIMS measurements indicate that the drop in carrier concentration observed in the capacitance characteristics must be due to both mechanisms: In dopant redistribution and crystal defect incorporation. The loss of In in the near-surface region of the substrate (0.2–1.0 μm) is insufficient to account for the large change in carrier concentration. However, the use of a pure H_2 ambient during the anneal leaves the Cd activity undefined due to the total absence of Cd in the H_2 atmosphere. Under such conditions, CdTe tries to provide the minimum Cd pressure required for its own phase stability at the given temperature to the adjacent gas phase. It is this loss of Cd from the substrate which results in the diffusion of Cd vacancies into the substrate. The inclusion of Cd vapor into the annealing atmosphere decreases the Cd loss from the substrate resulting in higher measured carrier concentration in the near-surface region. The Cd vacancy is one type of defect which is probably created as a result of the annealing treatment. Other defects, both acceptors and donors, may be and probably are generated during the anneal.

The crystal defects introduced into the CdTe substrate may also form deep levels in the energy gap of the semiconductor.[21] These defects can affect the capacitance measurements made on Schottky barrier devices, producing curvature in the capacitance plot, similar to that seen in Fig. 3. This curvature is dependent on the details of the measuring process and the energy and spatial distribution of such levels. Recent measurements, employing DLTS (deep level transient spectroscopy), on Au Schottky barriers formed on both H_2 annealed and unannealed CdTe indicate the presence of a

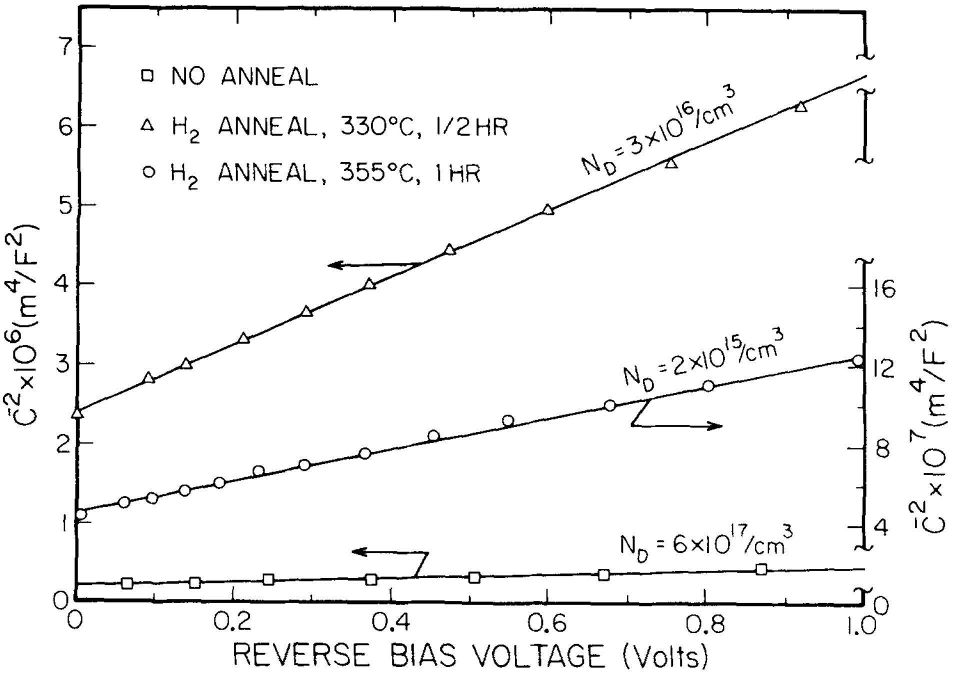

FIG. 5. Reverse bias capacitance measurements were made on Au Schottky barrier structures fabricated on CdTe substrate which had received varying annealing treatments. The carrier concentration deduced from the slope of the capacitance characteristic is indicated on each curve. The drop in carrier concentration observed in these structures is less than that found in HgTe/CdTe heterojunctions fabricated on similarly annealed substrates.

deep donor level located approximately 0.7 eV below the conduction band edge.[22] This level is near the Fermi level position found in the HgTe-CdTe heterojunction made using similarly annealed substrates. The concentration of the 0.7-eV level is, however, relatively insensitive to the annealing procedure and is also present in the unannealed substrate. No new deep levels are produced in the energy region 0.4 to 0.7 eV below the conduction band by H_2 annealing.[22]

B. Models of heterojunction behavior

We now consider models for the heterojunction which might fit the experimental observations just discussed. First there is the well-known defect model of Spicer *et al.*,[23] which postulates pinning of the Fermi level at the interface by states created by crystal defects. Next, we consider an inversion layer model, which postulates well-known MOS-transistor-like effects to explain the observations. Inasmuch as good quantitative agreement is not obtained by either simple model, we then discuss various modifications needed to be taken into account and propose further experiments.

Regarding the deep-level model, it should be noted that crystal defects are certainly present in CdTe, as evidenced by capacitance measurements, DLTS, and SIMS data. Deep levels associated with these defects could serve to pin the Fermi level in the HgTe-CdTe interface region. Changes in annealing procedure could alter the defect populations of the near-surface region of the CdTe. The presence of more than one deep level, each possessing a broad energy distribution, could explain the continuous change in barrier height with annealing conditions exhibited in Fig. 4. In fact, however, the absence of substantial changes in the CdTe deep-level structure with annealing conditions, as discussed earlier, indicates that a deep-level defect model of Fermi level pinning is not applicable to the HgTe-CdTe heterojunction system.

An alternative view of the HgTe-CdTe heterojunction is afforded by a more detailed examination of the information obtained in the particular measurements we used. The "inversion model" proposed here will assume that the previously discussed predictions of a large barrier height are correct and that only a small valence band discontinuity exists. Such large Schottky barrier heights are uncommon and the conventional theory of Schottky barrier devices must be modified to take into account minority carriers. The effect of minority carriers becomes more pronounced as the Schottky barrier height increases and the Fermi level is pushed closer to the valence band. The formation of an inversion layer may become possible depending on the bulk donor concentration and actual barrier height.

The presence of an inversion layer will substantially change the band bending in the semiconductor from that predicted from the simple model of a Schottky barrier. The band bending in the case considered here is found by solving Poisson's equation

$$\frac{d^2\phi}{dx^2} = -\frac{q}{\epsilon\epsilon_0}(N_D + p - n), \tag{5}$$

where N_D is the background donor doping and p and n are the hole and electron concentrations, respectively. The simple model of the Schottky barrier commonly discussed, the so-called "depletion approximation," excludes the effect of electrons and holes in the above equation. The solution of Eq. (5) for the case of an abrupt junction and uniform substrate doping was carried out here, following a treatment similar to that of Schwartz and Walsh.[24] The effect of minority carriers on the calculated band bending profile is easily seen in Fig. 6. The band profile given by the simple depletion layer Schottky model and that given by Eq. (5) are illustrated in the figure for a doping level of 10^{14} cm^{-3}. The zero of energy is taken to be the metal Fermi level and only the conduction band edge is shown. Since the Fermi level is near the valence band edge ($\phi \simeq E_{gap}$) in the CdTe, a high concentration of holes occurs in the CdTe near the interface. These

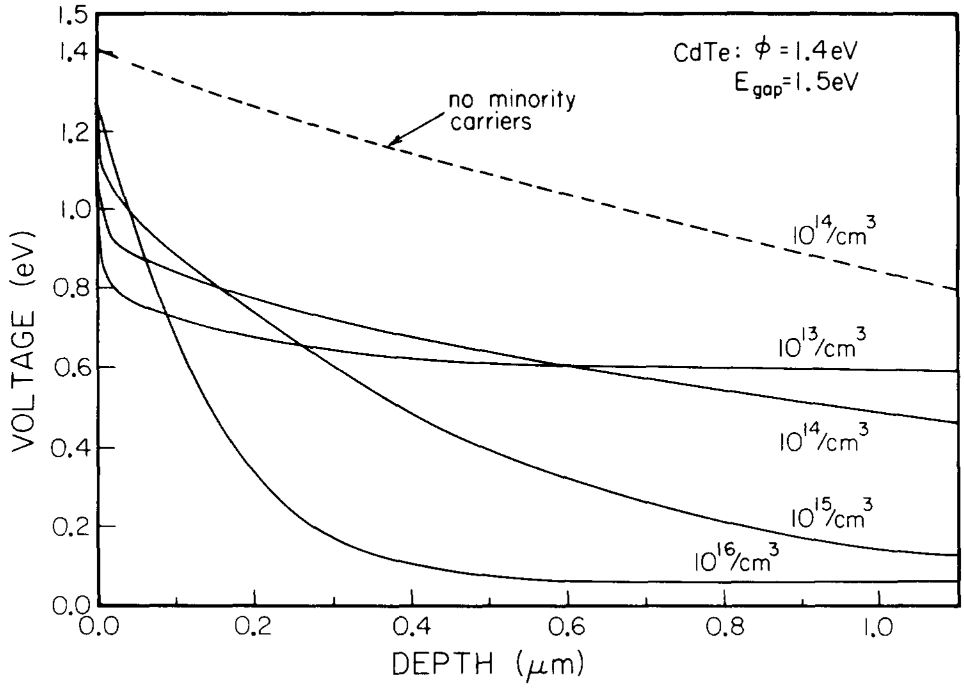

FIG. 6. Band-bending profiles for a large Schottky barrier height, $\phi = 1.4$ eV, structure on CdTe ($E_{gap} = 1.5$ eV) illustrates the influence of minority carriers in these devices. The zero of energy is taken to be the metal Fermi level with no applied bias. Only the conduction band is shown in the diagram. The lower four curves were calculated by means of Eq. (6) in order to include the effects of minority carriers on the band-bending profile using varying background doping levels. A band-bending profile calculated without inclusion of minority carriers is also shown. The band bending is very rapid beyond the resolution of this diagram, near the interface, due to the formation of an inversion layer which is only 50–100 Å in width.

holes cause very rapid band bending over a narrow region near the interface.

The influence of the inversion layer on the band-bending profile depends strongly on the semiconductor doping. The effect of minority carriers becomes more evident as the ratio of the donor concentration to the conduction band density of states decreases. An analogous situation is found in metal oxide semiconductor (MOSFET) transistors. The onset of inversion in the MOS structure approximately occurs when the applied bias causes the band bending to reach a value ϕ_{INV}:

$$q\phi_{INV} = E_{gap} - 2k_B T \ln [N_C/N_D], \tag{6}$$

where E_{gap} is the band gap energy, N_C is the conduction band density of states, and N_D is the fixed donor concentration.[25] The formation of an inversion layer occurs when the barrier height ϕ exceeds ϕ_{INV}. The excess voltage, V_{EX}, given by $V_{EX} = \phi - \phi_{INV}$ is then accommodated as a voltage drop over the inversion layer of the semiconductor, which appears in Fig. 6 as the very steep part of the voltage profile, particularly evident at low values of donor doping, e.g., 10^{13} cm^{-3}.

The rapid band bending occurring in a narrow region near the interface presents a potential spike through which electrons can easily tunnel, affecting the electrical measurements. Accordingly, the barrier height measured in the *I-V* and photoresponse technique becomes lower than the actual barrier height, due to this tunneling effect, and more like ϕ_{INV}. The deviation of the measured barrier height from the actual barrier would increase with reduction in the donor concentration, which is indeed what one sees in Fig. 4. If one assumes that the measured barrier height is proportional to ϕ_{INV}, the data points in Fig. 4 should have a slope of $2k_B T$ ln 10, as indicated. Furthermore, the capacitance characteristic would also exhibit deviations from that expected for the simple Schottky diode. The capacitance characteristic predicted by the inversion layer model exhibits a nonlinear behavior similar to that found in Fig. 3. It is difficult, however, to distinguish the capacitance curve deduced from the inversion model from that predicted for a structure with spatially varying deep levels.

The two models discussed above relate changes in heterojunction fabrication procedure to the measured barrier height and capacitance characteristic. The basic difference between the two models can be seen by noting the Fermi level position at the interface as the growth procedure is altered. In the deep-level model, the Fermi level position at the interface is changing with annealing conditions. The production of a new dominant deep level upon annealing would change the Fermi level and, hence, the Schottky barrier height. The second model states that while the barrier height is large and independent of the annealing conditions, it is our ability to measure the actual barrier height that is impaired by defect-related changes in the substrate material. Incidentally, the large barrier height postulated in the second model leaves this particular heterojunction an attractive possibility as a superlattice structure.

Of the two models discussed, the inversion layer model affords better agreement with observations. As is evident in Fig. 4, however, even for this model the agreement is not quantitative. Deviations from this model can be attributed to a few main effects. Spatial variations in the substrate doping can alter the influence of the inversion layer on the measured barrier height. There is the possibility of a high concentration of donor atoms being located near the HgTe-CdTe interface due to crystal defect donors or chemical impurity atoms (i.e., In). The present preliminary SIMS data does indicate a minor amount of In accumulation near the CdTe surface after annealing.

Also, the compositional grading present across the HgTe-CdTe interface will affect the measured barrier height by enhancing the effect of the minority carriers in the interdiffusion region, and leads to further decreases in the measured barrier height. The potential drop across the inverted layer, particularly in the interdiffused region of this heterojunction, would be underestimated by the application of the Boltzmann approximation to the solution of the electrostatic band-bending problem. This is particularly true in those spatial areas where interdiffusion has led to the formation of an alloy composition which is degenerate. Recent work by Kroemer[26] has shown that this is indeed the case for both Schottky barriers on degenerate semiconductors and *n-n* heterojunctions which exhibit the formation of an electron gas at the interface. Thus, the effect of interdiffusion and degeneracy in the interface region of this HgTe-CdTe heterojunction could substantially reduce the measured barrier height from that predicted by Eq. (6).

Other experiments on these structures could further distinguish between the two models. The change in electron transmission rates through the thin tunneling barrier should be evident in a sensitive photoresponse experiment. An accurate understanding of the internal photoemission data would require a more complete knowledge of the physical structure of the HgTe-CdTe interface and the resulting band-bending profile.[27] A more detailed study of the chemical profiles of Hg, Cd, and In across the metallurgical junction would be very useful in interpreting a wide variety of future experiments.

The attainment of barrier heights higher than those found in this study will require a greater control over the activities of all the chemical constituents present during the epilayer growth. This study has found that the substrate experiences a decrease in donor concentration not only during the annealing, but during the HgTe growth itself. This is seen by comparing Au Schottky barriers on appropriate annealed CdTe substrates. If this donor compensation can be attributed to a Cd loss from the substrate, the compensation occurring during the epilayer growth could be prevented by the growth of $Hg_{1-x}Cd_xTe$ instead of pure HgTe. The growth of $Hg_{1-x}Cd_xTe$ fixes the Cd activity in the epilayer, thus inhibiting defect-related effects from occurring during the epilayer growth. $Hg_{1-x}Cd_xTe$ remains a zero or negative band gap semiconductor for values of $x < 0.17$. The qualitative features of the lattice-matched Schottky barrier structure should be present in such structures.

The use of a lower temperature growth technique will also suppress the production and diffusion of defects during the fabrication of the heterojunction. The formation of HgTe-CdTe heterojunctions by use of molecular beam epitaxy (MBE) may permit crystal growth at temperatures below those used in the present CVD technique[28] and thus allow a more definitive study of this system.

VI. CONCLUSION

This study has provided the first measurements of the electrical properties of an abrupt HgTe-CdTe heterojunction. The lattice-matched Schottky barrier structure was grown by a new metal organic CVD technique which allows the epitaxial growth of HgTe on CdTe at low temperatures. The barrier height measured in these structures was found to be dependent on the details of growth procedure utilized. This dependence is most likely due to the formation of an inversion layer at the HgTe-CdTe interface. Such an inversion layer suggests that the valence band discontinuity between HgTe and CdTe is small, in agreement with previous theoretical estimates.

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